WHAT IS CLAIMED IS:

1. A processor comprising:

a first register configured to store a first target address;

a second register configured to store a second target address; and

an execution core coupled to the first register and the second register, wherein the execution core is configured, responsive to a first instruction, to: (i) select the first target address from the first register as a next program counter address if a first operating mode is active in the processor, and (ii) select the second target address from the second register as the next program counter address if a second operating mode is active in the processor.

2. The processor as recited in claim 1 further comprising a third register coupled to the execution core, a code segment register coupled to the execution core, and a stack segment register coupled to the execution core, wherein the execution core is configured, responsive to the first instruction, to: (i) read a first segment selector from the third register, (ii) store the first segment selector in the code segment register, and (ii) generate a second segment selector from the first segment selector and store the second segment selector in the stack segment register.

3. The processor as recited in claim 2 wherein the third register is further configured to store a third target address, and wherein the execution core is configured, responsive to the first instruction, to select the third target address as the next program counter address if a third operating mode is active in the processor.

4. The processor as recited in claim 1 wherein the first operating mode includes a default

address size greater than 32 bits.

5. The processor as recited in claim 1 further comprising a segment register configured to store a segment selector and at least a first operating mode indication and a second operating mode indication from a segment descriptor indicated by the segment selector, and still further comprising a configuration register storing an indication, wherein the processor is configured to generate an operating mode in response to the first operating mode indication, the second operating mode indication, and the indication in the configuration register.

6. The processor as recited in claim 1 further comprising a fourth register coupled to the execution core, wherein the execution core is configured to store a first address of a second instruction following the first instruction in the fourth register responsive to the first instruction.

7. The processor as recited in claim 6 wherein the execution core, responsive to a third instruction, is configured to branch to the first address, the processor further comprising a third register configured to store a first segment selector, and wherein the execution core is configured, responsive to the third instruction, to generate a second segment selector from the first segment selector responsive to an operand size of the third instruction.

8. The processor as recited in claim 7 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

9. The processor as recited in claim 7 wherein the second segment selector is equal to the first segment selector responsive to the operand size being 32 bit, and wherein the second segment selector is equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

10. The processor as recited in claim 9 wherein the execution core is configured to modify a first operating mode indication and a second operating mode indication stored in the segment register responsive to the operand size of the third instruction.

11. An apparatus comprising:

a first storage location corresponding to a first register, the first storage location storing a first target address;

a second storage location corresponding to a second register, the second storage location storing a second target address; and

a processor coupled to the first storage location and the second storage location, wherein the processor is configured, responsive to a first instruction, to: (i) select the first target address from the first storage location as a next program counter address if a first operating mode is active, and (ii) select the second target address from the second storage location as the next program counter address if a second operating mode is active.

12. The apparatus as recited in claim 11 further comprising a third storage location corresponding to a third register, a fourth storage location corresponding to a code segment register, and a fifth storage location corresponding to a stack segment register, wherein the processor is configured, responsive to the first instruction, to: (i) read a first segment selector from the third storage location, (ii) store the first segment selector in the fourth storage location, and (ii) generate a second segment selector from the first segment selector and store the second segment selector in the fifth storage location.

13. The apparatus as recited in claim 12 wherein the third storage location further stores a third target address, and wherein the processor is configured, responsive to the first

instruction, to select the third target address as the next program counter address if a third operating mode is active.

14. The apparatus as recited in claim 11 wherein the first operating mode includes a default address size greater than 32 bits.

15. The apparatus as recited in claim 11 further comprising a sixth storage location corresponding to a segment register, the sixth storage location storing a segment selector and at least a first operating mode indication and a second operating mode indication from a segment descriptor indicated by the segment selector, the apparatus still further comprising a seventh storage location storing an indication, wherein the processor is configured to generate an operating mode in response to the first operating mode indication, the second operating mode indication, and the indication in the seventh storage location.

16. The apparatus as recited in claim 11 further comprising an eighth storage location, wherein the processor is configured to store a first address of a second instruction following the first instruction in the eighth storage location responsive to the first instruction.

17. The apparatus as recited in claim 16 wherein the processor, responsive to a third instruction, is configured to branch to the first address, the apparatus further comprising a third storage location configured to store a first segment selector, and wherein the processor is configured, responsive to the third instruction, to generate a second segment selector from the first segment selector responsive to an operand size of the third instruction.

18. The apparatus as recited in claim 17 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

19. The apparatus as recited in claim 17 wherein the second segment selector is equal to the first segment selector responsive to the operand size being 32 bit, and wherein the second segment selector is equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

20. The apparatus as recited in claim 19 wherein the execution core is configured to modify a first operating mode indication and a second operating mode indication stored in the sixth storage location responsive to the operand size of the third instruction.

21. A method comprising:

selecting a first target address from a first register as a next program counter address responsive to a first operating mode during execution of a first instruction; and

selecting a second target address from a second register as the next program counter address responsive to a second operating mode during execution of the first instruction.

22. The method as recited in claim 21 further comprising, responsive to executing the first instruction:

reading a first segment selector from a third register;

storing the first segment selector in a code segment register;

generating a second segment selector from the first segment selector; and

storing the second segment selector in a stack segment register.

23. The method as recited in claim 22 wherein the third register is further configured to store a third target address, the method further comprising, responsive to the first instruction, selecting the third target address as the next program counter address during execution of the first instruction responsive to a third operating mode.

24. The method as recited in claim 22 wherein the first operating mode includes a default address size greater than 32 bits.

25. The method as recited in claim 21 further comprising generating an operating mode in response to a first operating mode indication, a second operating mode indication, and an indication in a configuration register, wherein a segment register is configured to store a segment selector and at least the first operating mode indication and the second operating mode indication from a segment descriptor indicated by the segment selector.

26. The method as recited in claim 21 further comprising storing a first address of a second instruction following the first instruction in a fourth register responsive to executing the first instruction.

27. The method as recited in claim 26 further comprising, responsive to a third instruction:

branching to the first address; and

generating a second segment selector from a first segment selector stored in a third register responsive to an operand size of the third instruction.

28. The method as recited in claim 27 wherein the operand size of the third instruction is

responsive to a prefix byte of the third instruction.

29. The method as recited in claim 27 wherein the generating comprises:

generating the second segment selector equal to the first segment selector responsive to the operand size being 32 bit; and

generating the second segment selector equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

30. The method as recited in claim 29 further comprising modifying a first operating mode indication and a second operating mode indication stored in the segment register responsive to the operand size of the third instruction.